



REMARK

Applicant respectfully requests reconsideration of this application as amended. Claims 7 and 12 have been amended; No Claims have been cancelled; and claims 16-18 have been added. Therefore, claims 1-3, and 7-18 are now presented for examination. Applicant submits that no new matter has been introduced.

U.S.C. §103(a) Rejections

The Examiner rejected claims 1,2,7-9,12,13 and 15 under 35 U.S.C. §103(a) as being unpatentable over Anderson (U.S. 5,905,910) and Jones et al. (U.S. 5,619,723). Applicant respectfully disagrees.

Claims 1-3 and 15-17 require, in some form or another,

"A striping disk controller and disk drive system for a computer system wherein said computer system includes a CPU connected to a system bus and executes an operating system including a BIOS, said striping disk controller and disk drive system comprising:
an interface connected to said system bus and communicating with said BIOS;
first and second disk drives each having data separator electronics, data formatting electronics and head positioning electronics;
a striping controller connected between said first and second disk drives and said interface, said striping controller

to cause data being communicated between said system bus and said first and second drives to be written to and read from said first and second drives in an interleaved form and substantially in parallel.

The claimed invention is concerned with allowing multiple disk drives to be accessed through a single IDE port using standard IDE drivers, thus eliminating unnecessary and expensive hardware as well as removing the necessity to rewrite the drivers for each operating system. The claimed invention accomplishes this by providing for an interface that communicates directly with the BIOS so that it can interpret a standard IDE driver contained in the BIOS and then, through the use of a striping controller, allow interleaved access to multiple IDE drives that contain standard electronics.

Two types of prior art are discussed at length in the disclosure.

The first, shown in Figure 2, shows a prior art where the BIOS of the host must be rewritten so that it can translate the sectors to meet IDE parameters of multiple IDE drives. This type of prior art requires that different IDE drivers be written for every operating system because the standard IDE drivers are insufficient to drive multiple IDE drivers. Anderson falls into this category, "The BIOS 106 translates the command from the operating system to generate data to select a cylinder, head, address, and the like on the selected disk drive. In response to this data, the selected disk drive will prepare for a data transfer by

positioning the read/write head (not shown) at the selected physical location on the disk drive and reading data into the internal buffer.” (See Col. 5, lines 44-50)

The second type of prior art discussed in the specification is shown in Figure 4. In this type of prior art, “the two IDE interfaces 50 and 52 are connected via busses 54 and 56 to striping controller 58. A microprocessor 60 is connected by bus 62 to striping controller 58. Microprocessor 60 runs the code that determines the types of striping action – e.g. interleaving the two disk drives to get better performance or mirroring for better redundancy. Buffer memory 64 stores some of the code for microprocessor 60 and acts as a cache for microprocessor 60. Microprocessor 60 is also interfaced to a host computer system across bus 66 such as ISA or PCI bus. The IDE electronics return status and error signals to microprocessor 60. Microprocessor 60 performs error correction and returns status and error messages to the host. Thus, part of the function of the microprocessor 60 is to manage the status and error signals from two different physical disk drives and report only one status and error to the host. The host believes that there is only one hard disk drive with twice the performance and twice the capacity, while in fact there are two disk drives that are interleaved. . . **Striping logic 58 performs the functions of translating the microprocessor 60 requests into the two physical IDE buses.** In this implementation, the disk drive does not look like an IDE drive to the host. Rather a disk access looks like a host to host communication. From an operating system perspective, **this means the standard IDE software driver cannot**

be used.” Jones, see Figure 1 and related discussion, falls into this type of prior art.

The Office Action correctly recognizes the failure of Anderson to “specifically teach an interface connected to the system bus and communicating with the BIOS; and a striping controller causing data being communicated between said system bus and said first and second drives to be substantially read or written in parallel.” However, the Office Action then incorrectly interprets Jones as teaching an interface that communicates directly with the BIOS. In demonstrating the second type of prior Art Jones is teaching a host to host communication where the local processor 102 must still have rewritten IDE driver instructions in its BIOS to handle multiple IDE drives. From the Office Action discussion, it appears that the bus interface 108 is being equated with the interface of the claimed invention. However, from an operating system perspective the functionality of a system bus is extremely different from the interface of the claimed invention. The claimed invention requires that the “interface connected to the system bus,” communicates with the BIOS of the operating system contained on a CPU on the other side of the bus. This claim language is saying that a standard IDE interface may be used to receive the instructions from the BIOS. Jones does not teach or suggest that the bus interface communicates with the BIOS of the other CPU. In fact, any discussion of a BIOS is referring to the local processor. Rather, the bus interface allows the local processor 102 to access the system bus when communicating with another

CPU. Because the Office Action fails to address how Jones teaches the elements admittedly missing from Anderson, specifically, "an interface connected to said system bus and communicating with said BIOS," any combination of Jones and Anderson would also fail to teach all of the elements of the claimed invention.

Additionally, a combination of Anderson and Jones is not obvious because it would teach away from the independent patents. In Anderson, as in Figure 2 of the invention, the BIOS translates sectors to IDE parameters and then directs them to multiple IDE drives. In contrast, Jones teaches a bus interface that receives a general instruction, uses a local processor to determine which IDE drives are to be used and then breaks the message down for the IDE drives. To combine Anderson and Jones would destroy the purpose of each. To take a message from Anderson that has already been translated into sectors and IDE parameters and transmit that to another CPU to further break down sectors when it has already been accomplished creates unnecessary redundancy and would provide no additional benefit as the information has already been prepared to go to specific IDE drives. Similarly, Jones is based on the assumption that a single instruction is received and it then breaks down the instruction into multiple IDE drives in order to provide error protection.

Claims 7, 12-14 and 18 require, in some form or another, "receiving at a striping controller an IDE system request intended for a single physical drive from the system bus," and then interpreting that IDE system request to interleave data on two drives. Again, this is not taught in Anderson or Jones. In

Anderson, each drive receives its own system requests which are not interpreted for multiple drives and in Jones, the CPU receives a host-to-host communication that is not an IDE system request for disk access. Consequently, any combination of Anderson and Jones fails to teach or render obvious the claimed invention.

Claims 8-11 require, in part, "control logic connected with said interface to cause data being communicated via said system bus to be written to and read from a first and a second disk drive in an interleaved form and substantially in parallel." Neither Anderson or Jones teach or suggest control logic to perform this function. Rather Anderson teaches a BIOS that separates the segments and then instructs individual IDE drives to receive these segments and Jones teaches a CPU that receives a storage request and then, using RAM, ROM and CPU instructions, directs the data to various IDE drives. There is teaching or suggestion to use control logic to perform these functions.

The Examiner rejected claims 3, 10 and 14 under 35 U.S.C. §103(a) as being unpatentable over Anderson (U.S. 5,905,910) and Jones et al. (U.S. 5,619,723) and if further view of Jenkins (U.S. 4,047,157). Applicant disagrees with this rejection for at least the reasons stated above.

Additionally, with reference to all rejections, Applicant maintains arguments presented in prior responses and arguments for redress on Appeal if necessary.



Conclusion

Applicant respectfully submits that the objection and rejections have been overcome by the Amendment and Remark, and that the claims as amended are now in condition for allowance. Accordingly, Applicant respectfully requests the objection and rejections be withdrawn and the claims as amended be allowed.



Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

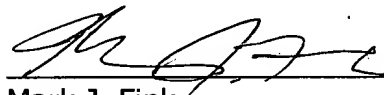
Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: April 4, 2001



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Version With Markings To Show Changes Made

In the claims:

7. (Amended) A method of writing data onto two disk drives using a striping controller connected to system bus, said method comprising:

receiving at a striping controller [a] an IDE system request intended for a single physical drive from the system bus; and

writing to and reading from a first and a second drive in an interleaved form and substantially in parallel in response to said IDE system request.

12. (Amended) An apparatus for writing data onto two disk drives connected to system bus, said apparatus comprising:

means for receiving [a] an IDE system request intended for a single physical drive from the system bus; and

means for writing to and reading from a first and a second drive in an interleaved form and substantially in parallel in response to said IDE system request.

16. (New) A system comprising:

a central processing unit (CPU) connected to a system bus and

executing an operating system including a Basic Input/Output

Operating System (BIOS);

an IDE interface connected to the system bus and communicating with the BIOS;

a striping controller connected between the IDE interface and a first storage and a second storage, wherein the striping controller, based on a standard IDE driver instruction, causes data being communicated to be written to and read from the first and second storage in an interleaved form and substantially in parallel.

17. (New) The system of claim 16, wherein the striping controller comprises an exclusive-or gate; a first FIFO memory driven by a signal from the exclusive-or gate to access the first storage and a second FIFO memory driven by the signal inverted from the exclusive-or gate to access the second storage.
18. (New) A method comprising: receiving a standard IDE driver instruction intended for accessing a single IDE disk drive and interpreting the standard IDE driver instruction such that data associated with the standard IDE driver instruction is interleaved between a first IDE disk drive and a second IDE disk drive.